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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,283	12/30/2003	Andrew Crosland	15114H-071500US	2380

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,283	CROSLAND ET AL.	
	Examiner	Art Unit	
	Don P. Le.	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 7/27/04.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Bapat et al. (US 5,847,580).

3. With respect to claim 1, figures 4-18 of Bapat discloses a programmable logic device, comprising a plurality of logic elements (CLBs) and a routing structure, wherein the routing structure comprises a plurality of routing Lines, and wherein each routing Line comprises:

a plurality of first OR gates (85a ..85d, figure 14), each first OR gate having at Least a first input connected to a respective one of said Logic elements in a first group of said Logic elements, and each first OR gate except a final first OR gate in said Line having an output connected to a second input of a respective succeeding one of said first OR gates, such that a signal from one of said Logic elements in the first group of Logic elements appears on an output of the final first OR gate in said Line; and

connections to a plurality of said Logic elements in a second group of Logic elements, such that the signal appearing on said output of the final first 0R gate in said line may be passed to said plurality of Logic elements in the second group of Logic elements (examiner interpretation of logic grouping is any two CLB can be considered a group of CLBs).

4. With respect to claim 2, the grouping of CLBs can be exclusive.

5. With respect to claim 3, the CLB of Bapat contains at least one Logic element in common.

6. With respect to claim 4, the logic elements of Bapat are arranged in an array, the array comprising rows and columns of Logic elements.

7. With respect to claims 5-14, the grouping of elements can be interpreted as any two or more CLBs are grouped together. There is no clear boundary where the CLBs can be located.

8. With respect to claims 15-17, figures 34-18 of Bapat disclose a programmable logic device, comprising:

a plurality of Logic elements (CLBs) arranged in an array, the array comprising rows and columns of Logic elements, the rows of said array being located at respective vertical positions in said array, and the columns of said array being located at respective horizontal positions in said array; and

a routing structure, wherein the routing structure comprises a first plurality of routing lines (programmable interconnect contains many lines), running parallel to said rows of Logic elements at a first vertical position in said array; a second plurality of routing Lines, running parallel to said rows of Logic elements at a second vertical position in said array; a third plurality of routing Lines, running parallel to said columns of logic elements at a first horizontal position in said array; and a fourth plurality of routing Lines, running parallel to said columns of Logic elements at a second horizontal position in said array,

wherein each routing Line comprises:

a plurality of first OR gates (85a..85d, figure 14), each first OR gate having at Least a first input connected to a respective one of said logic elements in a respective first group of said

Logic elements, and each first OR gate except a final first OR gate in said Line having an output connected to a second input of a respective succeeding one of said first OR gates, such that a signal from one of said Logic elements in the first group of logic elements appears on an output of the final first OR gate in said line; and

connections to a plurality of said Logic elements in a respective second group of Logic elements, such that the signal appearing on said output of the final first OR gate in said line may be passed to said plurality of Logic elements in the second group of Logic elements.

9. With respect to claims 18-20, the methods therein are inherent given the apparatus of Bapat as shown in the above rejections.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7/29/2005

DON LE
PRIMARY EXAMINER